WHAT IS CLAIMED IS:

1. A method for fabricating transistors of different conduction types arranged in a first section of a surface of a semiconductor substrate with a high packing density and in a second section with a low packing density, comprising:

providing a gate electrode having a doping of a first conduction type on the semiconductor substrate at least in the first section;

producing encapsulated gate structures assigned to the transistors in the first and second sections, the gate structures having gate electrodes emerging from the gate electrode layer and cover structures emerging from a second dielectric layer provided above the gate electrode layer;

providing a spacer structure perpendicular to the surface of the semiconductor substrate and comprising a third dielectric layer for the encapsulation of the gate structures, the gate structure sections of the second dielectric layer which are formed as a cover structure remaining in the gate structures during the formation of the spacer structures and the cover structure and the spacer structure comprising materials that can be removed selectively with respect to one another;

using the encapsulated gate structures as a protective mask and/or conductive structure for auxiliary structures for a self-aligning contact-connection of the transistors in the first section;

applying a protective layer in the region of the first section;

opening encapsulated gate structures arranged in the second section by selective removal of the cover structures, thereby uncovering at least a portion of the gate electrodes; and

simultaneously doping, in each case, the gate electrode and assigned source/drain regions of at least a first subset of transistors arranged in the second section, with a dopant for a second conduction type opposite to the first conduction type, so that in each case the source/drain

regions and the gate electrode of a transistor arranged in the second section are provided in each case with a doping of the same conduction type.

2. The method as in claim 1, wherein

a first dielectric layer is provided on the surface of the semiconductor substrate,

the gate electrode layer is applied to the first dielectric layer, and

the gate electrode layer is doped with a dopant for the first conduction type at least in the first section.

3. The method as in claim 1, wherein the gate electrode layer is doped with the dopant for the first conduction type exclusively in the first section, and
the gate electrodes of transistors of the first and second conduction types arranged in the second section are uncovered.

4. The method as in claim 1, wherein the gate electrode layer is provided with the dopant for the first conduction type in the first section and a first partial region of the second section, and the gate electrodes of transistors that are to be provided of the second conduction type and are arranged in the second section are uncovered.

5. The method as in claim 1, wherein a contact layer is provided on the gate electrode layer doped in sections and is removed for the purpose of uncovering the gate electrodes in the second section.

6. The method as in claim 1, wherein for the purpose of uncovering the gate electrodes, the contact layer is removed by means of a selective wet etching process.

7. The method as in claim 1, wherein after the doping of the gate electrodes and the formation of the source/drain regions,

a layer made of a metal is applied at least in the second section,

the metal is heated, a first portion of the metal reacting in the region of the gate electrodes with a material of the gate electrode and in the region of the uncovered sections of the semiconductor substrate with a material of the semiconductor substrate to form a patterned silicide layer and

a second portion of the metal, not contained in the patterned silicide layer, is removed.

8. The method as in claim 1, wherein isolation trenches which isolate the source/drain regions of mutually adjacent transistors from one another are provided in the second section in the semiconductor substrate.

9. The method as in claim 1, wherein for the encapsulation of the gate structures,

a second dielectric layer is applied to the contact layer,

the gate electrode layer, the contact layer and the second dielectric layer are patterned and the gate structures are produced in the process, and

a third dielectric layer is provided on sidewalls of the gate structures which are inclined or vertical with respect to the surface of the semiconductor substrate.

10. The method as in claim 9, wherein

the third dielectric layer is provided in a manner extending over partial sections provided for the self-aligning contact-connection on the semiconductor substrate.

11. The method as in claim 1, wherein during a doping of the source/drain regions with a dopant for the first conduction type in the first section, partial sections provided for the self-aligning contact-connection on the semiconductor substrate are spared.

12. The method as in claim 1, wherein

auxiliary structures are provided for the self-aligning contact-connection in the first section,

a fourth dielectric layer is applied to the first and to the second section, and

the fourth dielectric layer is patterned in the second section in such a way that the third dielectric layer formed at the sidewalls of the gate structures is reinforced by the fourth dielectric layer.

13. The method as claimed in claim 1,

wherein for the application of the protective layer,

an etching stop layer is deposited, and

the etching stop layer is patterned by means of a mask in such a way that the etching stop layer is removed above the second section.

14. A method for fabricating transistors of different conduction types arranged in a first section of a surface of a semiconductor substrate with a high packing density and in a second section with a low packing density, comprising:

providing a gate electrode having a doping of a first conduction type on the semiconductor substrate at least in the first section;

producing encapsulated gate structures assigned to the transistors in the first and second sections, the gate structures having gate electrodes emerging from the gate electrode layer and cover structures emerging from a second dielectric layer provided above the gate electrode layer;

providing a spacer structure perpendicular to the surface of the semiconductor substrate and comprising a third dielectric layer for the encapsulation of the gate structures, the gate structure sections of the second dielectric layer which are formed as a cover structure remaining in the gate structures during the formation of the spacer structures and the cover structure and the spacer structure comprising materials that can be removed selectively with respect to one another; and

simultaneously doping, in each case, the gate electrode and assigned source/drain regions of at least a first subset of transistors arranged in the second section, with a dopant for a second conduction type opposite to the first conduction type, so that in each case the source/drain regions and the gate electrode of a transistor arranged in the second section are provided in each case with a doping of the same conduction type.

15. A method for fabricating transistors of different conduction types arranged in a first section of a surface of a semiconductor substrate with a high packing density and in a second section with a low packing density, comprising:

providing a gate electrode having a doping of a first conduction type on the semiconductor substrate at least in the first section;

producing encapsulated gate structures assigned to the transistors in the first and second sections, the gate structures having gate electrodes emerging from the gate electrode layer and cover structures emerging from a second dielectric layer provided above the gate electrode layer; and

providing a spacer structure perpendicular to the surface of the semiconductor substrate and comprising a third dielectric layer for the encapsulation of the gate structures, the gate structure sections of the second dielectric layer which are formed as a cover structure remaining in the gate structures during the formation of the spacer structures and the cover structure and the spacer structure comprising materials that can be removed selectively with respect to one another.